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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/478,714	01/06/2000	TONY S. EL-KIK	BAYS-10-8-2	2054

8933 7590 06/03/2004

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	19

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/478,714	EL-KIK ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-8,10 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8,10 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4-8, 10, and 14-16 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #18. Amendment "E" as received on 4/6/2004.

Withdrawn Rejections

3. Applicant has overcome, through amendment, the rejections set forth in the Office Action mailed on December 24, 2003, which are hereby withdrawn by the examiner. However, upon further consideration, a new ground(s) of rejection is made below.

Claim Objections

4. Claim 1 is objected to because of the following informalities: In the last line on page 2, applicant claims "...the data register reads data words at the consecutive memory locations..." The examiner asserts that a register does not have the ability to read data. Instead it merely stores data that has been written to it so that it may be read in the future. Consequently, applicant should reword this portion of the claim. Appropriate correction is required.

5. Claim 5 is objected to because of the following informalities: In the last paragraph on page 4, applicant claims "...the data register reads data words at the one or more consecutive memory blocks..." The examiner asserts that a register does not have the ability to read data. Instead it merely stores data that has been written to it so that it may be read in the future.

Consequently, applicant should reword this portion of the claim. Appropriate correction is required.

6. Claim 10 is objected to because of the following informalities: Please replace "means_reads" with --means reads-- in the second to last paragraph. Also, in the second to last paragraph on page 6, applicant claims "...the data register means reads data words at the consecutive memory locations..." The examiner asserts that a register means does not have the ability to read data. Instead it merely stores data that has been written to it so that it may be read in the future. Consequently, applicant should reword this portion of the claim. Appropriate correction is required.

7. Claim 16 is objected to because of the following informalities: Remove "and" from the phrase "and a memory bank field". Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 1, 4-8, 10, and 14-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In each of the independent claims, applicant claims that the burst transfers are accomplished "independent of a count (number) of words to be exchanged (transferred)" between the first and second processors.

The examiner asserts that if the transfer were completely independent of the number of words to be exchanged, the first processor would never know when to stop transferring (when to de-assert the data register system address). More specifically, one of the two processors, in this case, the main processor, would have to inherently know how many data words that it needs to transfer. If it does not know the number of words, then it will also not know when to stop transferring. As a result, applicant should clarify this limitation by claiming something along the lines of the coprocessor (second processor) not knowing the number of words to be transferred ahead of time.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claim 1 recites the limitation "said identified block" in the second paragraph. There is insufficient antecedent basis for this limitation in the claim. Possible language to correct this would be to replace "said identified block" with "one of said plurality of blocks identified by said block identifier".

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1, 4, 6-8, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Campanini, U.S. Patent No. 4,700,292 (as applied in the previous Office Action), in view of Harris, II et al., U.S. Patent No. 5,901,103 (herein referred to as Harris), and further in view of Arimilli et al., U.S. Patent No. 5,109,490 (herein referred to as Arimilli).

14. Referring to claim 1, Campanini has taught a dual processor system, comprising:

a) a first processor coupled to a system address bus and a data bus. See Fig.1 and note that a first processor EL_A is coupled to a bus BC, which is used to transmit both data and addresses to a second processor EL_B. For instance, during burst transfer, both a starting address is passed along BC to the second processor (making it an address bus in that it passes addresses) and the actual data to be transferred will eventually follow (making a data bus in that it passes data).

b) a second processor coupled to the system address bus and to the data bus (See Fig.1, component EL_B), the second processor comprising:

b1) a control register having a control register system address. Note the control register comprises the MEA and WCA storage locations in Fig.5. Both of these locations control the second processor during transfer mode. Also, note that these registers are read from and written to for increment and decrement purposes, respectively (see column 9, lines 27-34). Therefore, in order to read and write to specific locations, the control registers must be addressable.

b2) an internal memory. See Fig.1, components DIS_B and MED_B. Campanini has not explicitly taught that the internal memory is partitioned into a plurality of blocks each having a known number of addressable memory locations. However, Harris has taught such a concept. See Fig.1 and note that the internal memory has been divided into blocks

26, 28, 30, 32, and 34. Also, it is inherent that memories have a known number of addressable locations, as the number of locations is finite and therefore known. A partitioned memory allows for the enabling (and supplying power to) only those memory blocks that are currently being accessed. See the abstract. Harris has further taught that by supplying power to only those banks which require it, the user is given some control over the system's power consumption and more flexibility in distributing power is achieved. In general, power dissipation can be reduced by not powering memory banks that are not being used. See column 2, line 52, to column 3, line 23. Consequently, in order to reduce unnecessary power consumption, it would have been obvious to one of ordinary skill in the art at the time of the invention to partition Campanini's internal memory so that only those partitions which are being used are enabled (and powered) by the system, as taught by Harris.

b3) a data register having a data register system address and coupled to the internal memory. See Fig.4, and note the REI register. This data register receives all incoming words where the words are then propagated to the buffer store (FIFO) and ultimately, to the appropriate destination within the internal memory. Also, note that the WR signal, which indicates a write is going to occur, is used to specify a word is being transferred. See column 9, lines 27-34. Therefore, the WR signal will act as a system address for the data register in that it results in the data register receiving some data. Note also that this data register is coupled to the internal memory since the internal memory is the final destination for the transferred words.

b4) and an internal address generator coupled to the control register and to the internal memory. See column 9, lines 26-34. Note that the MEA control register initially holds the starting internal memory address. This address is incremented by an internal address generator each time a new word is being transferred to memory.

c) a control word is written into the control register when the first processor places a control word having a burst mode bit and a starting address within said identified block on the data bus and asserts the control register system address on the system address bus. Note that header data is sent prior to the actual data words that are to be transferred. See the abstract. This header includes the number of words to be transferred and the starting destination address. See column 2, lines 33-38, and column 8, line 61, to column 9, line 10. Note that the control register is addressed appropriately, such that the word count is put in the WCA control register and the starting address is put in the MEA register. Addresses need to be provided in order to select one of these registers. Note that the word count, stored in the WCA register, includes a burst mode indication. If the word count is stored as an X-bit number, then the X-1 most significant bits are the burst mode indicators. If any one of those bits is set to 1, then that bit is a burst mode bit. This can be seen with a simple example. Suppose, one word is to be transferred (non-burst mode) and the word count is appropriately set to 00000001 (where X=8). The seven (X-1) most significant bits are set to 0, indicating that the processors are not in burst transfer mode. However, if three words were to be transferred and the word count were set to 00000011, then it can be seen that one of the seven most significant bits is set to 1, indicating burst mode. Therefore, that bit would be a burst mode bit. Campanini has not taught writing a block identifier to the control register. However, recall from above that it would have been obvious to

partition Campanini's memory to save power (in view of Harris). If only the accessed block is being powered, then that block must be identified, as taught by Harris in Fig.5, component 102.

d) the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting address, during subsequent data transfer cycles, when said burst mode is indicated and so long as the first processor asserts the data register system address on the system address bus. See column 9, lines 24-38. As long as the counter is greater than zero and was initially greater than one, burst mode is indicated, and data words will be transferred.

e) in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the consecutive memory locations. See column 9, lines 24-38. Basically, the first processor asserts the WR signal, specifying a write to the data register and then transfers the data word to be written. This word will then be stored at the address specified by the MEA register, where the value of this register is incremented for as many words that are to be transferred, which is specified by the WCA register. Campanini has not taught that the burst mode transfer is independent of a count of words to be exchanged. However, Arimilli has taught such a concept. See column 4, lines 39-58. Arimilli states that by not using a counter for storing a count of words to be exchanged, a block length does not need to be defined in advance, thereby reducing the amount of work that would be required by Campanini's system before the transfer is performed. In addition, a person of ordinary skill in the art would have recognized that by eliminating this counter, a transfer of

any size could be performed since it the number of data words is not constrained to a limiting counter size. In addition, Arimilli has stated that his system is analogous to the counter system (of Arimilli), and therefore, for this reason and the previous reasons, it would have been obvious to one of ordinary skill in the art to remove the counter in Campanini and perform burst transfers in the fashion taught by Arimilli.

f) in a read burst mode, the first processor asserts the data register system address on the system address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, and the data register reads data words at the consecutive memory locations and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor. See column 9, lines 24-38, and column 1, lines 7-10, and note that the relationship between processors is interchangeable, i.e., the first processor can be the sender or the receiver. In this situation, when the first processor is to receive from the slave, this would be read mode, and it would work much like the write mode mentioned above. Campanini has not taught that the burst mode transfer is independent of a count of words to be exchanged. However, for the same reasoning set forth in part (e) above, it would have been obvious to one of ordinary skill in the art to remove the counter in Campanini and perform burst transfers in the fashion taught by Arimilli.

15. Referring to claim 4, it has been noted by the examiner that claim 1 includes all limitations claimed in claim 4. Therefore, claim 4 is rejected for the same reasons set forth in the rejection of claim 1 above. In addition, Campanini has taught many selectable devices such as other coprocessors (see Fig.1, note that different memories may be selected as well as a

coprocessor), a data bus (see Fig.1, component BC), a chip select line (see Fig.2 and note the AK signal. This signal results in the activation (selection) of the REI chip. See column 6, lines 47-55), a read signal line (see Fig.2 and note the RY signal, which signifies that the second processor is ready to read transferred data. See column 6, lines 39-44), and a write signal line (see Fig.2 and column 9, lines 24-38 and note that the WR signal is used to signify a write operation).

16. Referring to claim 6, Campanini in view of Harris and further in view of Arimilli has taught a dual processor system as described in claim 1. Campanini has further taught that the second processor is a co-processor. See column 1, lines 29-43 and note that the second processor (slave) will assist the main processor if the main processor malfunctions or even if it doesn't malfunction (as described in column 3, lines 26-28).

17. Referring to claim 7, Campanini in view of Harris and further in view of Arimilli has taught a dual processor system as described in claim 1. Since the counter of Campanini, and therefore Campanini's single burst indicator has been eliminated, Arimilli has taught that the second processor enters a single data transfer mode in which the internal address generator selects the starting internal address specified in the control word stored in the control register, and the data is transferred from the first processor to a specified location into memory of the second processor during a next data transfer cycle when the control word has a burst mode bit that does not indicate burst mode. Note that the S0,S1 (read/write) signal acts as a single burst indicator in some instances. See Fig.5, column 8, lines 60-68, and column 10, lines 66-68. For instance, from Fig.5, it should be realized that the S0,S1 signal is in the low state. When it, goes high, then the transfer will stop after the current data word is completely transferred. Therefore,

for single transfer mode, while one data word is being transferred, the S0,S1 signal will be negated and the transfer will be completed after the current word is finished transfer. When not using a counter, this is the type of indicator that is used to indicate a transfer of one or more words.

18. Referring to claim 8, Campanini in view of Harris and further in view of Arimilli has taught a dual processor system as described in claim 1. Campanini has further taught that the first processor and second processor are intercoupled by:

a) the system address bus and the data bus to select a co-processor in a system having many selectable devices such as other co-processors. Recall from the rejection of claim 1 that the BC bus shown in Fig.1 is a system data/address bus. Also, note from Fig.1, that multiple devices, such as mass memory, working memory, and interface chip, and coprocessor.

b) a chip select line. See Fig.2 and note the AK signal. This signal results in the activation (selection) of the REI chip. See column 6, lines 47-55.

c) a read signal line. See Fig.2 and note the RY signal, which signifies that the second processor is ready to read transferred data. See column 6, lines 39-44.

d) a write signal line. See Fig.2 and column 9, lines 24-38 and note that the WR signal is used to signify a write operation.

19. Referring to claim 16, Campanini in view of Arimilli has taught an integrated circuit as described in claim 10. Campanini has not explicitly taught:

a) the internal memory comprises a plurality of memory blocks wherein data are stored in consecutive locations. However, Harris has taught such a concept. See Fig.1 and note that the internal memory has been divided into blocks 26, 28, 30, 32, and 34. Also, it is inherent that

memories have a known number of addressable locations, as the number of locations is finite and therefore known. A partitioned memory allows for the enabling (and supplying power to) only those memory blocks that are currently being accessed. See the abstract. Harris has further taught that by supplying power to only those banks which require it, the user is given some control over the system's power consumption and more flexibility in distributing power is achieved. In general, power dissipation can be reduced by not powering memory banks that are not being used. See column 2, line 52, to column 3, line 23. Consequently, in order to reduce unnecessary power consumption, it would have been obvious to one of ordinary skill in the art at the time of the invention to partition Campanini's internal memory so that only those partitions which are being used are enabled (and powered) by the system, as taught by Harris.

b) Campanini has taught that the control word comprises an internal bank address field which specifies the starting internal bank address within the selected memory bank. Recall that the starting address is written to the MEA register. See column 8, lines 54-58. Campanini has not taught that the control word comprises a memory bank field which specifies a selected memory bank of the plurality of memory banks. However, recall from above that it would have been obvious to partition Campanini's memory to save power (in view of Harris). If only the accessed block is being powered, then that block must be identified, as taught by Harris in Fig.5, component 102. Finally, Campanini has not taught that the control word comprises a burst mode bit field. However, note that the S0,S1 (read/write) signal of Arimilli acts as a burst mode bit. See Fig.5, column 8, lines 60-68, and column 10, lines 66-68. For instance, from Fig.5, it should be realized that the S0,S1 signal is in the low state. As long as the signal stays low, a burst of data can be transferred. Since Campanini's counter has been eliminated in view of Arimilli's

non-counter system, this is the type of indicator that is used to indicate that a burst of words may be transferred.

20. Claims 5, 10, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Campanini, as applied above, in view of Arimilli, as applied above.

21. Referring to claim 5, it has been noted by the examiner that claim 1 includes all of the limitations claimed in claim 5 except that claim 1 claims a partitioned memory whereas claim 5 includes just an "internal memory". Therefore, although claim 5 is rejected for the same reasons set forth in claim 1, the Harris reference relied upon in the rejection of claim 1 is not needed in the rejection of claim 5 since Campanini has taught a non-partitioned internal memory (Fig.1). In addition, Campanini has taught many selectable devices such as other coprocessors (see Fig.1, note that different memories may be selected as well as a coprocessor), a data bus (see Fig.1, component BC), a chip select line (see Fig.2 and note the AK signal. This signal results in the activation (selection) of the REI chip. See column 6, lines 47-55), a read signal line (see Fig.2 and note the RY signal, which signifies that the second processor is ready to read transferred data. See column 6, lines 39-44), and a write signal line (see Fig.2 and column 9, lines 24-38 and note that the WR signal is used to signify a write operation).

22. Referring to claim 10, it has been noted by the examiner that the only differences between claim 1 and claim 10 is that claim 10 does not claim a partitioned memory. Therefore, although claim 10 is rejected for the same reasons set forth in claim 1, the Harris reference relied upon in the rejection of claim 1 is not needed in the rejection of claim 10 since Campanini has taught a non-partitioned internal memory (Fig.1).

23. Referring to claim 14, Campanini in view of Arimilli has taught an integrated circuit as described in claim 10. Furthermore, it has been noted by the examiner that the only difference between claim 6 and claim 14 is that claim 6 claims a dual processor system while claim 14 claims a multiprocessor system. However, a dual-processor system is a multi-processor system. Consequently, claim 14 is rejected for the same reasons set forth in the rejection of claim 6.

24. Referring to claim 15, Campanini in view of Arimilli has taught an integrated circuit as described in claim 10. Furthermore, it has been noted by the examiner that the only difference between claim 8 and claim 15 is that claim 8 claims a dual processor system while claim 15 claims a multiprocessor system. However, a dual-processor system is a multi-processor system. Consequently, claim 15 is rejected for the same reasons set forth in the rejection of claim 8.

Response to Arguments

25. Applicant's arguments filed on March 10, 2004, have been fully considered but they are not persuasive.

26. In the remarks, Applicant argues the novelty/rejection of claim 1 on page 11 of the remarks, in substance that:

> "...in the present invention, there is no signal preceding each incoming data word. Rather, the mere presence of data on the address bus is sufficient to indicate that data is present."

27. This argument are not found persuasive for the following reasons:

a) Applicant's invention involves a data register address being asserted when a data word is to be written to the data register and ultimately transferred to memory. Asserting the data register address is similar to asserting the WR signal in Campanini. This signal indicates that a write is to occur to the data register for transfer.

28. In the remarks, Applicant argues the novelty/rejection of claim 1 on page 12 of the remarks, in substance that:

> "...using the word count concurrently as a word counter and a burst mode indicator would fail to maintain the co-processor in a burst mode when the word counter decreases to the value of 1."

29. This argument are not found persuasive for the following reasons:

a) The examiner asserts that if the value of 1 is written to the counter before the transfer begins, then the machine will be in single transfer mode, since only 1 data word will be transferred. However, when a value larger than 1 is written to the counter before the transfer begins, the system will be in burst mode, as multiple data items are to be transferred. Even when the counter decrements to 1 in burst mode, this means that there is just one data item left to transfer in the current burst. Furthermore, with applicant's amendments now excluding the count of words to be exchanged, this argument is somewhat moot, as the examiner is relying on a secondary reference (Arimilli) to show that a counter does not need to be used.

30. In the remarks, Applicant argues on page 12 of the remarks, in substance that:

> "...the examiner has further stated that because the claims use the open-ended term "comprising", the use of a word counter is not precluded from being included in the present invention. Under this logic, if a patent were obtained for a liquid containing the elements coffee, sugar, and milk, it would anticipate an application for a liquid containing only coffee, even if sugar and milk are not positively recited. The applicant submits that in this case, neither the claims nor the specification refer to the use of a word counter. Hence, there is no teaching that would encompass a word counter as being included in the novel concept of the present invention."

31. This argument are not found persuasive for the following reasons:

a) From MPEP §2111.03:

> "The transitional phrases "comprising", "consisting essentially of" and "consisting of" define the scope of a claim with respect to what unrecited additional components or steps, if any, are excluded from the scope of the claim.

> The transitional term "comprising", which is synonymous with "including," "containing," or "characterized by," is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. See, e.g., Genentech, Inc. v. Chiron Corp., 112 F.3d 495, 501, 42 USPQ2d 1608, 1613 (Fed. Cir. 1997) ("Comprising" is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim.); Moleculon Research Corp. v. CBS, Inc., 793 F.2d 1261, 229 USPQ 805 (Fed. Cir. 1986); In re Baxter, 656 F.2d 679, 686, 210 USPQ 795, 803 (CCPA 1981); Ex parte Davis, 80 USPQ 448, 450 (Bd. App. 1948) ("comprising" leaves "the claim open for the inclusion of unspecified ingredients even in major amounts")."

In summation, applicant is correct in saying that if a patent has been granted for a liquid with the elements milk, coffee, and sugar, then this patent would anticipate an application for a liquid "comprising" coffee, even if milk and sugar are unrecited in the application. In this case, coffee has already been taught by the patent, i.e., there is nothing new about the coffee itself. However, if applicant had a liquid comprising coffee, and some element X (where X is not milk or sugar), then the reference would not anticipate the application because it does not teach element X.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Yamashita et al., U.S. Patent No. 6,377,979, has taught a multiple-processor system and

method for transferring data and/or a program stored in one processor to another processor in order to process the data or to execute the program therein. A length of a data block (not a count of data words) is specified and used in transferring.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
May 20, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100